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PERFORMANCE ANALYSIS OF A LOW-POWER HIGH-SPEED HYBRID 1-BIT FULL ADDER CIRCUIT AND ITS IMPLEMENTATION

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ABSTRACT

In this paper, a hybrid low power and high speed 1-bit full adder design employing both complimentary metal oxide (CMOS) logic and transmission gate logic is reported. The design was implemented for 1 bit. The circuit was implemented using Mentor tanner tool in 180 and 90 nm technology. Performance parameters such as power, delay and transistor count were compared with existing designs such as complimentary pass transistor logic, transmission gate adder, transmission function adder, hybrid pass-logic with static CMOS logic output drive full adder , and so on. For 1.8-V supply at 180-nm technology, the average power consumption (0.40893 uW) was found to be extremely low with moderately low delay (7.0975 ps) resulting from the incorporation of strong transmission gates. Corresponding values of the same were 0.1265uW and 13.439ps at 90-nm technology operating at 1.2-V supply voltage.. In comparison with the existing full adder designs, the present implementation was found to offer significant improvement in terms of power and speed. The design was further extended for implementing 2 bit multiplier also as an application of our proposed design.

KEYWORDS: low power high speed transmission gate full adder application multiplier

I. INTRODUCTION

It is time we explore the well-engineered deep submicron CMOS technologies to address the challenging criteria of these emerging low-power and high-speed communication digital signal processing chips. The performance of many applications as digital signal processing depends upon the performance of the arithmetic circuits to execute complex algorithms such as convolution, correlation, and digital filtering. Fast arithmetic computation cells including adders and multipliers are the most frequently and widely used circuits in very-large-scale integration (VLSI) systems. The semiconductor industry has witnessed an explosive growth of integration of sophisticated multimedia-based applications into mobile electronics gadgetry since the last decade. However, the critical concern in this arena is to reduce the increase in power consumption beyond a certain range of operating frequency. Moreover, with the explosive growth, the demand, and the popularity of portable electronic products, the designers are driven to strive for smaller silicon area, higher speed, longer battery life, and enhanced reliability.

Adder is the core element of complex arithmetic circuits like addition. The XOR-XNOR circuits are basic building blocks in various circuits especially arithmetic circuits (adders & multipliers), compressors, comparators, parity checkers, code converters, error-detecting or error-correcting codes and phase detector. There are standard implementations with various logic styles that have been used in the past to design full-adder cells [1–4] and the same are used for comparison in this paper. Although they all have similar function, the way of producing the intermediate nodes and the transistor count is varied.

Different logic styles tend to favor one performance aspect at the expense of others. Standard static complementary metal–oxide–semiconductor (CMOS) , dynamic CMOS logic , complementary pass-transistor logic (CPL) and transmission gate full adder (TGA) , are the most important logic design styles in the conventional domain. The other adder designs use more than one logic style, known as hybrid-logic design style, for their implementation .These designs exploit the features of different logic styles to improve the overall performance of the full adder.

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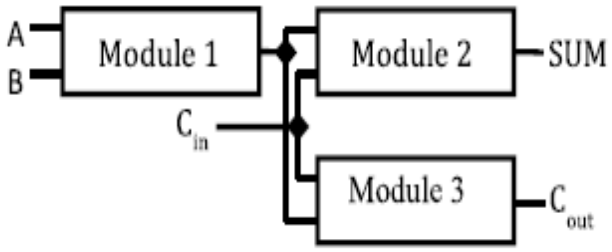
The advantages of standard complementary (CMOS) style-based adders (with 28 transistors) are its robustness against voltage scaling and transistor sizing; while the disadvantages are high input capacitance and requirement of buffers [3]. Another complementary type smart design is the mirror adder [4] with almost same power consumption and transistor count (as that of [3]) but the maximum carry propagation path/delay inside the adder is relatively smaller than that of the standard CMOS full adder. On the other hand, CPL shows good voltage swing restoration employing 32 transistors [5], [6]. However, CPL is not an appropriate choice for low-power applications. Because of its high switching activity of intermediate nodes (increased switching power), high transistor count, static inverters, and overloading of its inputs are the bottleneck of this approach. The prime disadvantage of CPL, that is, the voltage degradation was successfully addressed in TGA, which uses only 20 transistors for full adder implementation [7], [8]. However, the other drawbacks of CPL like slow-speed and high-power consumption remain an area of concern for the researchers. Later, researchers focused on the hybrid logic approach which exploited the features of different logic styles in order to improve the overall performance. Vesterbacka [10] reported a 14-transistor full adder employing more than one logic style for their implementation. Similarly, the hybrid pass logic with static CMOS output drive full adder (HPSC) was proposed by Zhang et al. [11]. In such HPSC circuit, XOR, and XNOR functions were simultaneously generated by pass transistor logic module by using only six transistors, and employed in CMOS module to produce f ollowing outputs of the full adder but at the cost of increased transistor count and decreased speed. Although the hybrid logic styles offers promising performance, most of these hybrid logic adders suffered from poor driving capability issue and their performance degrades drastically in the cascaded mode of operation if the suitably designed buffers are not included. The main aim of this paper is to improve the different performance parameters like power, delay and transistor count of the full adder compared with the already existing designs. The circuit was implemented using both 180- and 90-nm technology by using Mentor tanner tool. The average power consumption (0.40893 uW) of the proposed circuit was reduced dramatically by the proposed sum module coupled with strong transmission gates for carry module at 1.8 V supply when implemented at 180-nm technology. On the other hand, the delay of the circuit (7.0975 ps), in 180-nm technology, were comparable with the other hybridized implementations and better with respect to other full CMOS implementation, respectively. For 90-nm technology operated at 1.2-V power supply, the corresponding values are 0.1265uW (average power consumption), 13.439ps (delay). The design was extended and proved to be also promising for building a 2-bit multiplier.

II. DESIGN APPROACH OF PROPOSED FULL ADDER

The proposed full adder is represented by three blocks as shown in Fig .Module 1 and module 2 are the XNOR modules that generate the sum signal (SUM) and module 3 generates the carry output signal (Cout). Each module is designed individually such that the entire adder circuit is optimized in terms of power, delay and area. These modules are discussed below in detail.



Modified XOR Module

In the proposed full adder circuit , XOR module is responsible for most of the power consumption of the entire adder circuit. Therefore, this module is designed to minimize the power to the best possible extend with avoiding the voltage degradation possibility.

The sum output of the full adder is implemented by XOR modules. For the analysis of XOR structure the output signals are applied to the inputs to test the XOR gates with the values as AB=01 , AB=10,and AB= 11 were completed with good output signals. For an incomplete output signal, when applied the input signal to test the XOR gates with the values as AB=00, each PMOS will be on and will pass “LOW” signal level to the output

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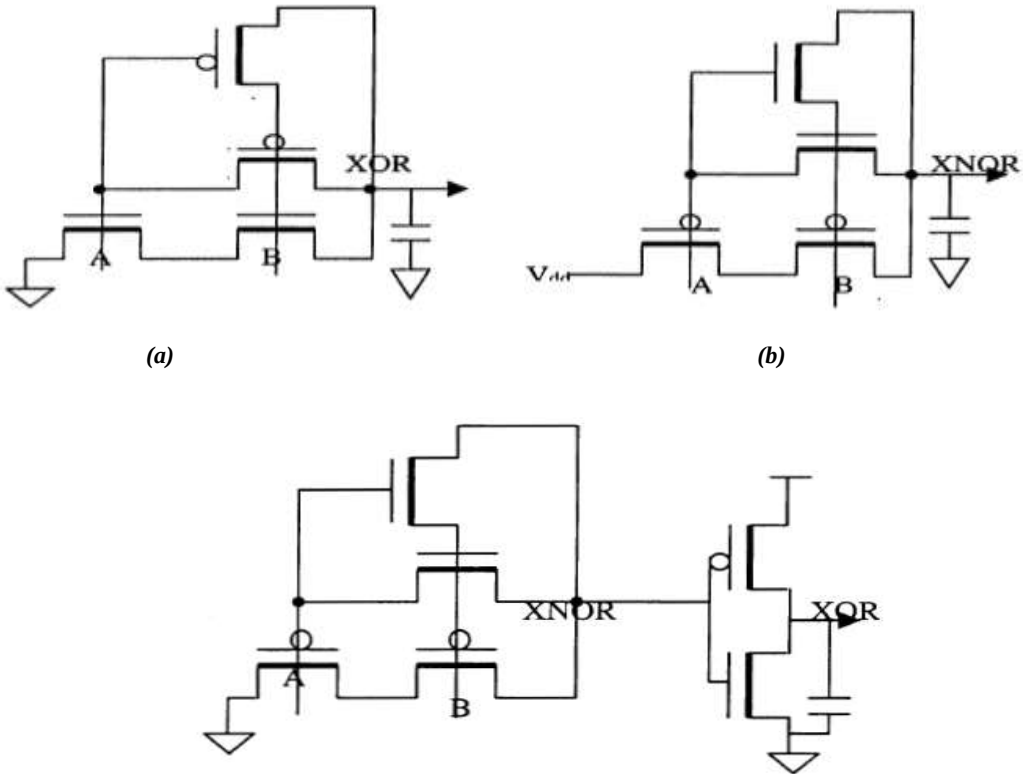
end. That is if the input signal to test the XOR gates with the values as AB=00, the output will have a threshold votage|Vpth|, a little higher than "LOW". For the XNOR function, the output signal incase of AB=00, AB=01, and AB=10 will be complete. When AB=11, each NMOS and pass the poor "HIGH" signal to the output end. By cascading an inverter to the XNOR structure, a new type of XOR structure which has a driving output and perfect signal in all cases is constructed.



(a) *(b)*

(c)

Fig. 1 a) XOR structure b) XNOR structure c) Schematic Structure of Sum Module

Carry Generation Module

In the proposed circuit, the output carry signal is implemented by transistors NMOS_5, PMOS_5 and NMOS_6 , PMOS_6 as shown in Fig .The input carry signal (Cin) propagates only through a single transmission gate (NMOS_5 and PMOS_5) , reducing the overall carry propagation path significantly. The deliberate use of strong transmission gates(channel width of transistors NMOS_5 , PMOS_5 , and NMOS_6 , PMOS_6 is made large) guaranteed further reduction in propagation delay of the carry signal.

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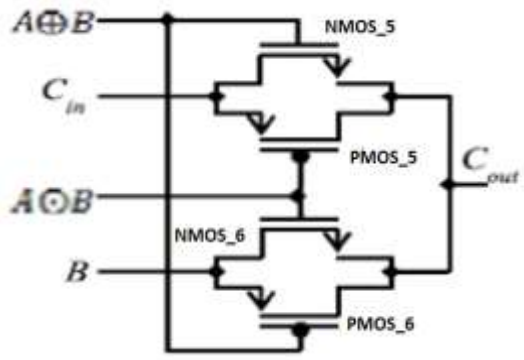

Fig. 2 Schematic Structure of Carry Module

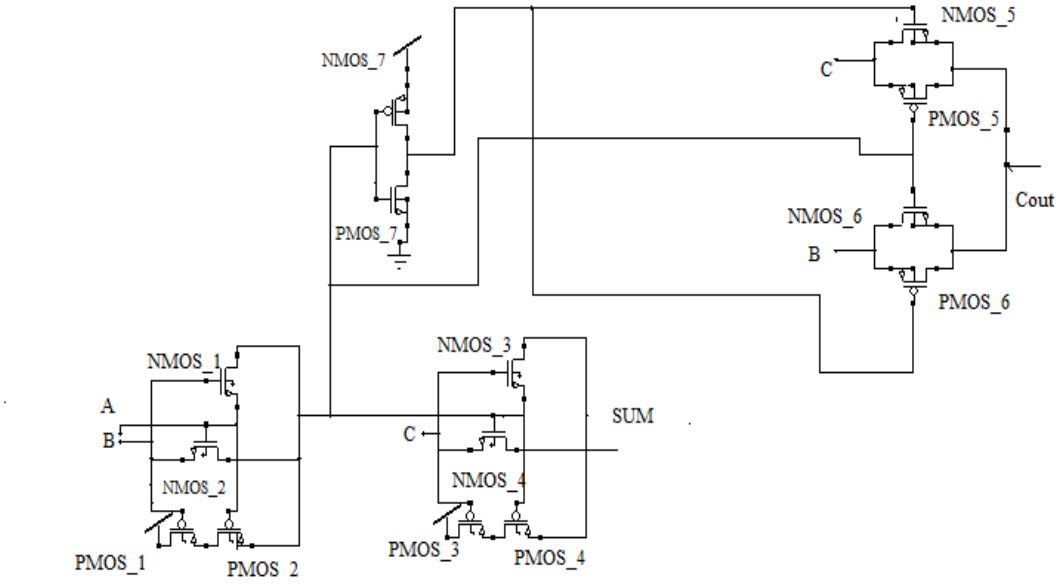

Fig 3. Detailed Circuit diagram of Proposed Full Adder

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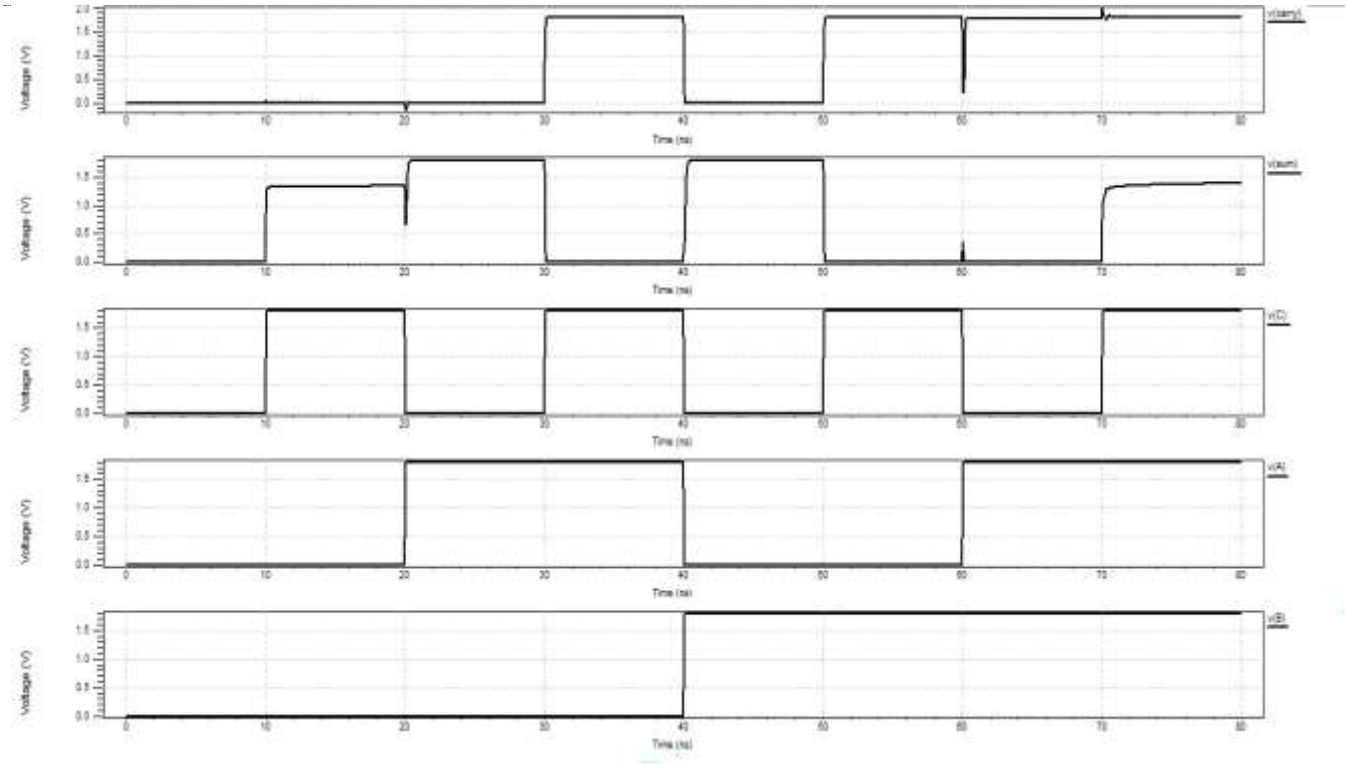

Fig 4. Output waveform of proposed full adder circuit

III. PERFORMANCE ANALYSIS OF PROPOSED FULL ADDER CIRCUIT

The simulation of the proposed full adder was carried out using both 90nm and 180nm technology and compared with the other potential adder designs reported in [1]–[11] and [15]–[24] with special emphasis on the hybrid design approach [1], [2], [19].

With an aim to optimize both power and delay of the circuit, the power-delay product (PDP), that is, the energy consumption has been minimized in the proposed case. It was observed that in the present design, the power consumption could be minimized by mainly sizing the transistors in inverter circuits; while the carry propagation delay could be improved by mainly sizing the transistors of the transmission gates present between the paths from C_{in} to C_{out}. The transistor sizes of the proposed full adder circuit are given in Table I for both the technologies (90 and 180 nm). Power consumption, propagation delay, and PDP of the proposed full adder along with that of existing full adders (from literature) are given in Tables II and III for 180-nm and 90-nm technology, respectively.

Table 1. Transistor size of proposed full adder

Transistor Name	180nm technology		90nm technology	
	Width(W) (nm)	Length(L) (nm)	Width(W) (nm)	Length(L) (nm)
PMOS_1,PMOS_2	200nm	180nm	200nm	180nm
NMOS_1,NMOS_2	180nm	180nm	180nm	180nm
PMOS_3,PMOS_4	200nm	180nm	200nm	180nm
NMOS_3	180nm	180nm	180nm	180nm
NMOS_4	500nm	180nm	180nm	180nm
PMOS_5, NMOS_5	180nm	400nm	400nm	180nm
PMOS_6,NMOS_6	400nm	180nm	400nm	180nm

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PMOS_7,NMOS_7	180nm	180nm	200nm	180nm

Table 2. Simulation Results for FULL ADDERS in 180nm Technology with 1.8V Supply

Design	Average Power(uW)	Delay(ps)	PDP(fJ)	Transistor Count	Reference
C-CMOS	6.2199	292.1	1.816832	28	[4,18]
Mirror	6.0797	281.61	1.712104	28	[18]
CPL	7.71985	183.97	1.4022	32	[5,6]
TFA	8.2491	287.1	2.368316	16	[21]
TGA	8.4719	293.9	2.8989	20	[7,8]
14T	12.7217	381.7	4.85587	14	[10]
10T	14.349	132.59	1.902062	10	[24]
HPSC	6.3798	273.7	1.74615	22	[11]
Majority Based	6.3227	185.4	1.7222	----	[23]
24T	15.91	314.2	4.998	24	[1]
FA_Hybrid	5.978	252.3	1.508	24	[2]
FA_DPL	19.56	226.6	4.432	22	[19]
FA SR-CPL	20.78	220.65	4.585	20	[19]
Other Hybrid	4.1563	224	0.931	16	[25]
Proposed	0.40893	7.0975	2.9024	14	[Present]

Table 3. Simulation Results for FULL ADDERS in 90nm Technology with 1.2V Supply

Design	Average Power(uW)	Delay(ps)	PDP(fJ)	Transistor Count	Reference
C-CMOS	1.5799	0.1269	0.200489	28	[4,18]
Mirror	1.5701	0.1226	0.19249	28	[18]
CPL	1.7598	0.0791	0.1392	32	[5,6]
TFA	1.7363	0.3198	0.55526	16	[21]
TGA	1.7619	0.2317	0.40823	20	[7,8]
14T	3.3297	0.3389	1.12843	14	[10]
10T	--------	-------	---------	10	[24]
HPSC	1.56	0.2207	0.34429	22	[11]
Majority Based	1.5751	0.0939	0.1479	----	[23]
24T	7.707	0.1406	1.0836	24	[1]
FA_Hybrid	6.21	0.143	0.888	24	[2]
FA_DPL	7.34	0.254	1.864	22	[19]
FA SR-CPL	7.4	0.167	1.235	20	[19]
Other Hybrid	1.17664	0.0913	0.107427	16	[25]
Proposed	0.1265	13.439	1.70	14	[Present]

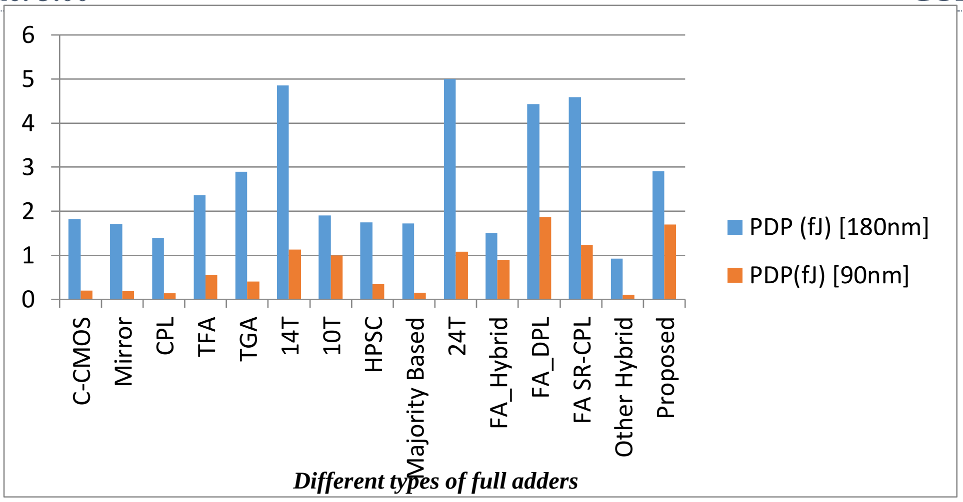

Fig 5. Comparison of PDP of various full adders

The proposed hybrid full adder has also been compared with other hybrid full adders reported in [1], [2], and [19].. The proposed hybrid adder requires only 14 transistors whereas the other hybrid adders [1], [2], [19] require more than 20 transistors. The average power consumed by the proposed full adder is significantly lower than that of other hybrid full adders. The use of less number of transistors in this paper also improved the speed. Because of reduction in average power consumption and propagation delay, the PDP of the proposed hybrid full adder is significantly improved in comparison with the earlier hybrid adders. The detailed comparison of the proposed full adder with other hybrid full adders [1], [2], [19] in 180- and 90-nm technology is represented in Tables II and III above, respectively.

IV. APPLICATION

Multipliers play an important role in today's digital signal processing and various other applications. With advances in technology, many researchers have tried and are trying to design multipliers which offer advantages like high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power and compact VLSI implementation .In this paper with the proposed adder circuit that provides sufficient low po wer and propagation delay, we have tried to build a multiplier circuit.

: Let us implement a two bit binary multiplier. Let the two binary numbers be a1a0 and x1x0. The multiplication table will, then,

```
                a1 a0
        X       x1  x0
---------------------------------------
                a1x0    a0x0
    a1x1    a0x1        X
-----------------------------------------------------------------------------------------
                P3  P2  P1  P0
```

Thus, we get the partial products as:

P0 = a0*x0

P1 = a0*x1 xor a1 * x0 ; carry generated here goes to next stage

P2 = a1*x1 xor (a0*x1) * (a1*x1)

P3 = a1*x1 and (a0*x1) * (a1*x0)

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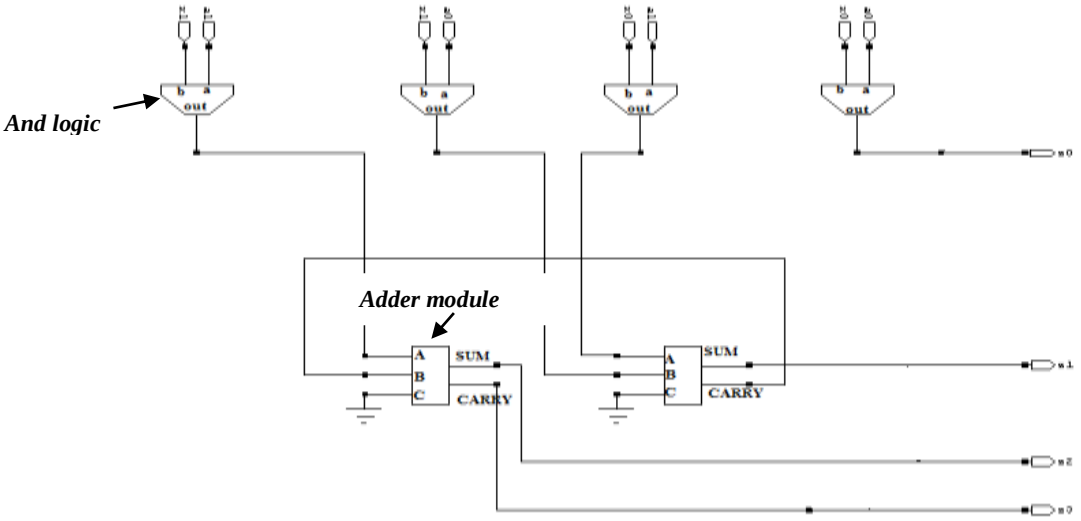

Fig 6. Multiplier circuit built with proposed adder circuit.

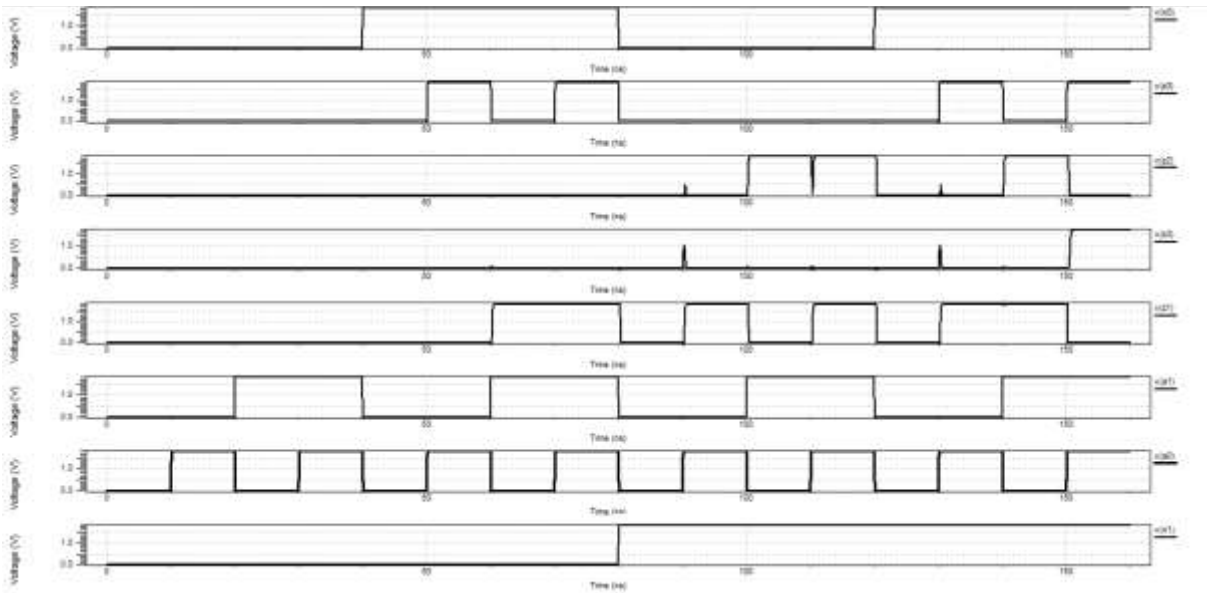

Fig 7. Output waveform for the multiplier circuit.

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